REMARKS

Applicants hereby submit this Request for Continued Examination so that the Examiner may consider the claims as modified herein. By this amendment, Applicants have canceled previously submitted claims 1-5. Claim 6 has been modified to further specify that the chips of the pseudo-wafer are bonded with each other via the protective material and furthermore that there is none of the protective material formed on the one surface at which the electrodes are formed, the electrodes being covered with a solder material for forming a solder ball.

Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to teach or suggest the subject matter of the invention as now specified. More specifically, the Brunet reference, United States patent number 6,420,211 merely describes a method for protecting an integrated circuit chip wherein insulating material may be applied by spraying, screen printing, dip coating or casting as described in the reference. Significantly, there is no teaching or suggestion whatsoever regarding the formation of a pseudo-wafer as described in the instant application.

More specifically, as described in the newly cited prior art, a protective coating is applied to a plurality of semiconductor chips that have been mounted on a support member 110. As described in column 4 beginning at line 50, integrated circuit chips 100 are cut out of a silicon wafer 10. The rear face 104 of the wafer is placed on adhesive 115 and the silicon wafer is then cut and the chips are thereafter placed on a support member 110. To the extent that the chips located on the support 110 could be considered a pseudo-wafer, there is simply no disclosure or suggestion whatsoever regarding bonding the adjacent chips together

via the protective material. Furthermore, there is no teaching or suggestion regarding the formation of solder bumps via the pseudo-wafer structure which is one of the key advantages of the present invention. In accordance with the present invention, the formation of solder-bumps is advantageously performed only on chips that have been verified to be good via a testing procedure which therefore eliminates the significant waste associated with the formation of these structures on defective chips. The prior art cited by the Examiner suffers from this deficiency. Accordingly, in light of the foregoing, Applicants respectfully submit that all claims now stand in condition for allowance.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-1794.

Respectfully submitted,

Date: 4/17/06

Robert J. Depke (Reg. #37,607)